PVP 20

Code: 20EC3302

II B.Tech - I Semester – Regular / Supplementary Examinations
DECEMBER 2022

DIGITAL LOGIC DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

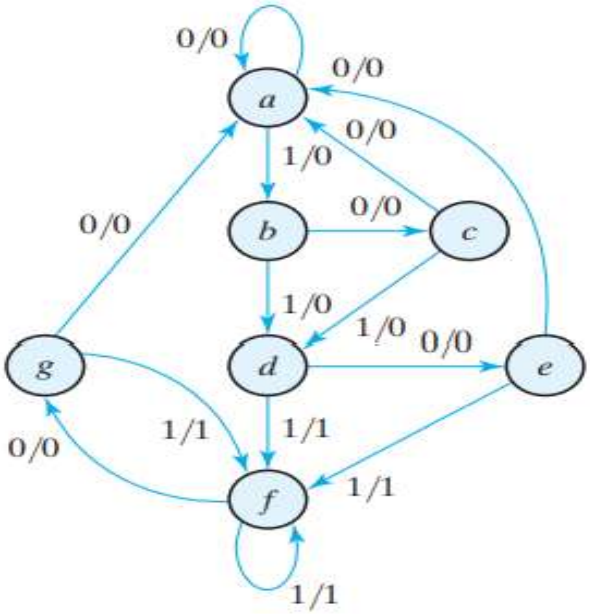
Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
		UNIT-I			
1	a)	Determine the base of the following number system if the given relations are valid. i) $\frac{33}{3}=11$ ii) $\sqrt{41}=5$	L2	CO1	6 M
	b)	Encode each of the 10 decimal digits 0, 1,..., 9 by means of the following weighted binary codes: 6 3 1 −1 7 3 2 −1 8 7 −4 −2 Determine which of the above codes is self-complementing.	L2	CO1	8 M
		OR			
2	a)	Convert BCD codes in to following codes. i) 2 4 2 1 ii) 6 4 2 -3	L2	CO1	6 M
	b)	State and Prove all theorems of Boolean algebra.	L2	CO1	8 M

		UNIT-II			
3	a)	Simplify the Boolean function using K-map and realize using multilevel OR- NAND, and AND-NOR F (w, x, y, z) = Σ m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)	L4	CO3	7 M
	b)	A safe has five locks, v, w, x, y, and z, all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner: A has keys for locks v and x; B has keys for locks v and y; C has keys for locks w and y; D has keys for locks x and z; E has keys for locks v and z. (i) Determine the minimum number of executives required to open the safe. (ii) Find all the combinations of executives that can open the safe. Write an expression f (A, B, C, D, E) which specifies when the safe can be opened as a function of which executives are present. (iii) Who is the "essential executive" without whom the safe cannot be opened?	L3	CO2	7 M
		OR			
4	a)	Given the function T(w, x, y, z)=Σ m(1, 2, 3, 5, 13) + Σ d (6, 7, 8, 9, 11, 15): (i) Find a minimal sum-of-products expression (ii) Find a minimal product-of-sums expression	L3	CO2	7 M
	b)	Simplify the following Boolean functions: i) $F_1(A, B, C, D) = \pi M(1, 3, 5, 7, 13, 15)$ ii) $F_2(A, B, C, D) = \pi M(1, 3, 6, 9, 11, 12,14)$	L3	CO3	7 M

UNIT-III					
5	a)	Design Full adder circuit with only NAND gates.	L4	CO4	7 M
	b)	Design a prime number detector for 4-bit input using i) 8×1 and ii) 4×1 Multiplexer	L4	CO4	7 M
OR					
6	a)	Design 4 Bit Parallel Adder / Subtractor and Explain.	L4	CO4	7 M
	b)	Design Four bit Binary to Gray Code Converter.	L4	CO4	7 M
UNIT-IV					
7	a)	Draw the neat diagram of SR flip flop and write the characteristic table.	L3	CO4	6 M
	b)	Design MOD-10 Synchronous counter using D-flip flops.	L4	CO5	8 M
OR					
8	a)	Convert JK flip flop to SR flip flop.	L4	CO4	6 M
	b)	Design 3 bit synchronous up/down counter.	L4	CO5	8 M

	UNIT-V			
9	Reduce the given state diagram and draw the reduced state diagram and suggest possible state assignment for each state.  	L4	CO5	14 M
	OR			
10	For following state table **Next State** / **Output** **Present State** | $x=0$ | $x=1$ | $x=0$ | $x=1$ a | f | b | 0 | 0 b | d | c | 0 | 0 c | f | e | 0 | 0 d | g | a | 1 | 0 e | d | c | 0 | 0 f | f | b | 1 | 1 g | g | h | 0 | 1 h | g | a | 1 | 0 i) Draw the corresponding state diagram. ii) Tabulate the reduced state table. iii) Draw the state diagram corresponding to the reduced state table.	L4	CO5	14 M